Appl. No. 10/605,745
Amdt. dated May 09, 2005
Reply to Office action of January 10, 2005

REMARKS

1. Objection to the specification:

5   All informalities identified by the Examiner and additional informalities identified in a
thorough review of the specification have been corrected. This includes eliminating extra
white-space and increasing the size of the equations. The changes are self-evident. No
new matter is entered. A likely source of these errors has been identified as the electronic
filing system.

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A copy showing changes made and a clean copy are provided.

Reconsideration of the specification is respectfully requested.

15   **2. Claim objections:**

In claim 2, the term "integernatural" is revised to "natural". Claim 11 has been cancelled.
Zero and negative scaling factors are not consistent with the disclosure.

20   In claims 1 and 10, "comprising following steps" is revised to "comprising the following
steps."

In claim 10, "portion data" is revised to "portion of data."

25   No new matter is entered by any of these amendments. Withdrawal of these objections is
respectfully requested.

3. Rejection of claims 2 and 11 under 35 U.S.C. 112, second paragraph:

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In claim 2, "natural number" is now recited. Claim 11 has been cancelled.

In claim 2, steps (a) and (b) are identified so as to make sense.

5 No new matter is entered by any of these amendments. Withdrawal of this rejection is respectfully requested.

4. Rejection of claims 1 and 8 under 35 U.S.C. 103(a) as being unpatentable over Nacman (US PGPub 2003/0128896) in view of Nishihaki et al. (JP 20001148997A):

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In the "Summary of Invention" one of the applicant's stated objectives is "to provide a method for scaling a digital picture with reduced memory." Accordingly, claim 1 is amended to expressly recite "for each different portion in sequence, repeating steps (a) and (b) to form the scaled picture" which is meant to further distinguish the serial-nature

15 of the invention from the parallel-nature of the cited art. This amendment adds no new matter.

The Examiner has asserted that processing images in parallel is functionally equivalent to the previously recited "repeating steps." While the end results may be similar, the

20 methods for obtaining those results are quite different. The amendment to claim 1 is meant to emphasize this difference.

Since an obviousness rejection requires a combination that teaches all limitations of the claims, and since neither Nacman nor Nishihaki teach or suggest serially scaling portions

25 of an image (Nishihaki expressly teaches parallel scaling), this rejection should be withdrawn.

Moreover, given the cited art, one of ordinary skill in the art would not arrive at the invention as recited in amended claim 1. The motivation provided by the Examiner

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("faster image scaling") necessarily results in parallel scaling. One or ordinary skill in the art would likely fully recognize the speed advantage of Nishihaki, in fact, they probably wouldn't even consider this art if high-speed scaling was not of interest. Thus, the applicant argues that there is no motivation to make the combination of Nacman and

5 Nishihaki to achieve serial scaling as now unequivocally recited in claim 1. Rather, the serial scaling concept goes against Nishihaki's teachings.

Reconsideration of claims 1 and 8 is requested in view of the amendment to claim 1. Claim 8 is dependent and should be allowed if claim 1 is allowed.

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5. Rejection of claims 2-4 under 35 U.S.C. 103(a) as being unpatentable over Nacman in view of Nishihaki as applied to claim 1 above, and further in view of Van Asma et al. (US 6,600,514 B1):

15 Reconsideration of claims 2-4 is requested in view of the amendment to claim 1. Claims 2-4 are dependent and should be allowed if claim 1 is allowed.

6. Rejection of claims 5-7 under 35 U.S.C. 103(a) as being unpatentable over Nacman in view of Nishihaki as applied to claim 1 above, and further in view of

20 **Nielsen (US 6,591,011 B1):**

Claims 6 and 7 are amended to narrow the recited general mirroring to a localized mirroring that is actually a boundary condition of the filter. The mirror boundary condition was recited in the original disclosure and no new matter is entered. This

25 boundary condition further refines the invention by allowing for higher quality scaled images even when buffer size is substantially limited.

While Nielsen teaches mirroring images, Nielsen does not teach or suggest a mirror boundary condition in a filter.

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Reconsideration of claims 5-7 is requested in view of the amendments to claims 1, 5, and 7. Claims 5-7 are dependent and should be allowed if claim 1 is allowed.

5   **7. Rejection of claim 9 under 35 U.S.C. 103(a) as being unpatentable over <u>Nacman</u> in view of <u>Nishihaki</u> as applied to claim 1 above, and further in view of <u>Iga</u> (US PGPub 2004/0021790 A1):**

Claim 9 is amended to amend the recited removal of part of the picture to omitting part of

10   the picture, which the applicant asserts more narrowly defines the decimation of extra rows/columns of an image in down-scaling recited in the original disclosure. No new matter is entered.

<u>Iga</u>, on the other hand, teaches noise removal, which cannot reasonably be read as

15   "omitting part of the digital picture."

Reconsideration of claim 9 is requested in view of the amendments to claims 1 and 9. Claim 9 is dependent and should be allowed if claim 1 is allowed.

20   **8. Rejection of claims 10 and 16 under 35 U.S.C. 103(a) as being unpatentable over <u>Masaki</u> (US PGPub 2003/0218774 A1) in view of <u>Nacman</u>:**

Claim 10 is amended to be consistent with the amended claim 1, that is, a new step (h) is added to emphasize the serial processing aspect of the invention.

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Although without further amendment claim 10 would stand with the amended claim 1 and should be patentable over the cited art as claim 1 is asserted to be, claim 10 is further amended to emphasize another aspect of the invention. Specifically, the filter used is recited as having L taps and the sizes of the portions of data are limited to correspond to L.

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This was described in the first paragraph of the "Detailed Description" of the original disclosure, thus, no new matter is entered.

5   Accordingly, claim 11 is cancelled to avoid redundancy. The variable L is preferred over N in claim 10 since it directly corresponds back to the disclosure. Furthermore, L is inherently a natural number since zero or negative sizes or taps are illogical or redundant. Hence, the term "natural number" is omitted from claim 10.

10   The combination of Masaki and Nacman requires processing by two filters, one for each direction. There is no suggestion in either art that one filter can be used. Rather, Nacman discloses one processor for each direction (i.e. two processors 22 and 24), and Masaki discloses two filters (i.e. FIL3 and MAG 5). Thus, having made the combination of Nacman and Masaki, one of ordinary skill in the art would not recognize that the combination could be reduced to a single filter.

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In addition, there is no suggestion in Asma (from rejection of claim 11) to limit image data to specific sizes corresponding to the filter taps.

20   Therefore, the amended claim 10 includes limitations that are not taught or suggested by the cited art, and are further not obvious due to the omission of a second filter.

These are not trivial differences, in fact, they allow for distinct advantages of the invention, namely, to allow "horizontal-scaling and vertical-scaling processes to use the same number of filter taps for achieving the best possible quality, while the buffer

25   memory requirement is kept to be as small as possible and is proportional to the filter length." (second last paragraph of "Detailed Description".)

Reconsideration of claims 10 and 16 is requested in view of the amendment to claim 10. Claim 16 is dependent and should be allowed if claim 10 is allowed.

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9. Rejection of claims 11-13 under 35 U.S.C. 103(a) as being unpatentable over Masaki in view of Nacman as applied to claim 10 above, and further in view of Asma:

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Claim 11 has been cancelled.

Reconsideration of claims 12 and 13 is requested in view of the amendment to claim 10. Claims 12 and 13 are dependent and should be allowed if claim 10 is allowed.

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10. Rejection of claims 14 and 15 under 35 U.S.C. 103(a) as being unpatentable over Masaki in view of Nacman as applied to claim 10 above, and further in view of Nielsen:

15   Claims 14 and 15 are amended to narrow the recited general mirroring to a localized mirroring that is actually a boundary condition of the buffer and filter. The mirror boundary condition was recited in the original disclosure and no new matter is entered. This boundary condition further refines the invention by allowing for higher quality scaled images even when buffer size is substantially limited.
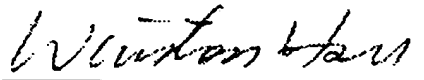
20

While Nielsen teaches mirroring images, Nielsen does not teach or suggest a mirror boundary condition in a buffer or filter.

Reconsideration of claims 14 and 15 is requested in view of the amendments to claims 10,

25   15, and 15. Claims 14 and 15 are dependent and should be allowed if claim 10 is allowed.

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Respectfully submitted,

Winston Hsu   Date: __May 9, 2005__

5   Winston Hsu, Patent Agent No. 41,526

P.O. BOX 506, Merrifield, VA 22116, U.S.A.

Voice Mail: 302-729-1562

Facsimile: 806-498-6673

e-mail : winstonhsu@naipo.com

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Note: Please leave a message in my voice mail if you need to talk to me. The time in D.C.
is 12 hours behind the Taiwan time, i.e. 9 AM in D.C. = 9 PM in Taiwan).

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CLEAN COPY OF THE SPECIFICATION

The entire specification is presented:

5   Background of Invention

1. Field of the Invention

The present invention relates to scaling digital pictures, and more particularly, to scaling digital pictures with reduced memory usage.

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2. Description of the Prior Art

In practice, scaling digital pictures is usually performed for still images or video frames to fit a specific application. The conventional method to scale a picture is to scale its horizontal dimension (width) first and then its vertical dimension (height), or vice

15   versa. This requires a large buffer memory to store the results of scaling the horizontal dimension.

Please refer to Fig. 1 and Fig. 2. Fig. 1 is a schematic diagram of an up-scaling process according to the prior art, and Fig. 2 is a schematic diagram of a down-scaling

20   process according to the prior art. W_{old} and H_{old} are the old width and old height; W_{new} and H_{new} are the new width and new height; SRC is a memory for storing a source picture; DST is a memory for storing a scaled picture; and BUFFER is a memory for temporarily storing data during the scaling process. The method for performing a scaling process is to use the sampling formula at a new sampling point as Eq. 1.

25     $$x(t) = \sum_{n=-i}^{j} x(n)h(t-n) \qquad \text{(Eq. 1)}$$

Where x(t) is the new pixel value at the new sampling point t from n=0, x(n) is the original pixel value at index n, and h(t-n) is the value of an interpolation function shifted

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by t from index n. Furthermore, the coefficients i and j give the number of original pixels involved in reconstructing x(t), i.e. the number of original pixels involved is given by (i+j+1). As a result, based on Eq. 1, the scaling process can be realized by a filter-bank implementation. The number (i+j+1) gives the number of filter taps and h(n) is the tap

5   weighting at n. The sampling process and the theory behind it are well known by those in the art, and accordingly it will not be discussed in detail here.

Ideally, a large buffer memory provides the freedom for a scaling process to exploit filters of any length to achieve the required scaling quality. That is, the size of the buffer

10   memory required is $(W_{new}*H_{old})$ bytes. However, from Fig. 1 and Fig. 2, the problem is when up-scaling the input picture the memory required increases dramatically. For example, if a picture is to be scaled to be two times larger in each dimension, the buffer memory required becomes $(W_{new}*H_{old})=(2*W_{old}*H_{old})$. This high memory requirement is not feasible in some applications. In particular, this high memory requirement is not

15   suitable for hardware implementation by integrated circuits (ICs).

Summary of Invention

It is therefore a primary objective of the claimed invention to provide a method for

20   scaling a digital picture with reduced memory to solve the above-mentioned problem.

According to the claimed invention, a method for scaling a digital picture comprising following steps:(a) inputting a source picture to a source memory; (b) providing a first buffer and a second buffer; (c) determining scaling factors; (d)

25   generating initial data in the first buffer and second buffer; (e) transferring a portion data of the digital picture from the source memory to the first buffer; (f) using a filter to scale the data in the first buffer in a first direction and storing the scaled data in the second buffer; (g) using the filter to scale the data in the second buffer in a second direction and storing the scaled data in a destination memory; and (h) outputting a scaled picture from

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the destination memory.

These and other objectives of the present invention will no doubt become obvious to those of ordinary skill in the art after reading the following detailed description of the

5   preferred embodiment that is illustrated in the various figures and drawings.

Brief Description of Drawings

Fig. 1 is a schematic diagram of an up-scaling process according to the prior art.

10   Fig. 2 is a schematic diagram of a down-scaling process according to the prior art.

Fig. 3 is a schematic diagram of an up-scaling process according to the present invention.

Fig. 4 is a schematic diagram of a down-scaling process according to the present invention.

Fig. 5 is a flowchart according to the present invention.

15   Fig. 6 is a flowchart of a preferred embodiment according to the present invention.

Fig. 7 is a schematic diagram of mirrored data extension.

Detailed Description

20   Please refer to Fig. 3 and Fig. 4. Fig. 3 is a schematic diagram of an up-scaling process according to the present invention, and Fig. 4 is a schematic diagram of a down-scaling process according to the present invention, where SRC is a memory for storing a source picture, and DST is a memory for storing a scaled picture. The size of the first line-buffer BUFFER1 is $(m*W_{old})$ bytes and the size of the second-buffer BUFFER2

25   is $(n*W_{new})$ bytes, where m and n are the number of lines for the first and second buffers and depend on the length of the filter used. That is, if the length of the interpolation filter is L, then $m = L$ and $n = (2*L-1)$. Furthermore, the function of the buffer BUFFER1 is to store data needed for horizontal scaling as well as to store the decimated picture data. The BUFFER1 is not necessary if the source picture can be randomly accessed from the

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memory SRC. On the other hand, the function of the BUFFER2 is to store the horizontally scaled results as well as to organize the data for vertical scaling.

Please refer to Fig. 5. Fig. 5 is a flowchart according to the present invention. In step
5   210, the picture to be scaled is inputted and stored in the memory SRC. In step 220, the scaling operation for the picture is determined as being up-scaling or down-scaling. If the picture is to be up-scaled, during step 221, rows of picture data are transferred to the buffer BUFFER1. If the picture is to be down-scaled, during step 222, the data decimation operation is determined. If the decimation operation is enabled, rows of the
10   picture data are decimated when necessary and transferred to the buffer BUFFER1. Otherwise, rows of picture data are transferred to the buffer BUFFER1. In step 230, the horizontal scaling process is performed and the results are stored in the buffer BUFFER2. In step 240, the vertical scaling process is performed and the results are outputted to the memory DST. In step 250, if the picture has data remaining to be scaled, repeat step 220
15   to step 240 until all rows of the picture data have been horizontally and vertically scaled. Finally, the step 260 is executed to finish the scaling process.

Please refer to Fig. 6. Fig. 6 is a flowchart of a preferred embodiment according to the present invention. For clearly explaining the spirit of this invention, the preferred
20   embodiment of this invention exploits a 4-tap interpolation filter to perform the scaling process. Furthermore, the up-scaling ratio is assumed to be up to twice as large as the original picture in each dimension, but the down-scaling ratio is not limited. Therefore, the size of the buffer BUFFER1 is $4*W_{old}$ bytes and the size of the buffer BUFFER2 is $7*W_{new} = 14*W_{old}$ bytes, as $W_{new} = 2*W_{old}$. For conveniently explaining the processing
25   steps in the flowchart, the whole process can be divided into three groups, namely the initialization steps, horizontal scaling steps, and vertical scaling steps.

In the group of initialization steps, the picture to be scaled is firstly inputted and stored in the memory SRC. After that, the scaling factors and the decimation factors are

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determined. Initially, the horizontal and vertical scaling factors are respectively given by $S_h = W_{old}/W_{new}$ and $S_v = H_{old}/H_{new}$, where W_{old} and H_{old} are respectively the width and height of the input picture, and W_{new} and H_{new} are respectively the width and height to be scaled to. The initial horizontal scaling factor S_h determines whether the picture data will

5   be decimated in the horizontal direction before being transferred to the buffer BUFFER1. That is, if the decimation operation is enabled and $S_h > 2$, then picture data is decimated horizontally according to the horizontal decimation factor $d_h = floor(log_2 S_h)$, where the floor function truncates the decimal portions; otherwise, no horizontal data decimation will be performed and set $d_h = 0$. Similarly, the initial vertical scaling factor S_v

10   determines whether the picture data will be decimated in the vertical direction before being transferred to the buffer BUFFER1. That is, if the decimation is enabled and $S_v > 2$, then picture data is decimated vertically according to the vertical decimation factor $d_v = floor(log_2 S_v)$; otherwise, no vertical data decimation will be performed and set $d_v = 0$. As a result, according to the picture decimation process, the data in the memory BUFFER1

15   and the memory SRC can be generally expressed as:

$$BUFFER1(x,i) = SRC(2^{dh} * x, 2^{dv} * (y+i)),$$

where x ranges from 0 to $(W_{old}-1)$, y ranges from 0 to $(H_{old}-1)$ and i ranges from 0 to 3.

Since after decimation the width and height of the input picture will become $W_d =$

20   W_{old}/d_h and $H_d = H_{old}/d_v$, the actual scaling factors used in the scaling process are referred to as $S_h = W_d/W_{new}$ and $S_v = H_d/H_{new}$. After determining the decimation and scaling factor, the initial horizontal scaling process is preformed. In this process, two lines of SRC data are transferred to the buffer BUFFER1, such as:

$$BUFFER1(x,0) = SRC(2^{dh} * x, 0),$$

25   $$BUFFER1(x,1) = SRC(2^{dh} * x, 2^{dv}),$$

where x ranges from 0 to (W_d-1).

Based on Eq. 1, the initial horizontal scaling process on these two lines of data becomes:

$$BUFFER2(x2,5) = \sum_{n=-1}^{2} BUFFER1(x1 + n, 0) * w(n), \text{ and}$$

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$$BUFFER2(x2,6) = \sum_{n=-1}^{2} BUFFER1(x1 + n,1) * w(n)$$

where $x2$ ranges from 0 to $(W_{new}-1)$ and $x1 = floor(S_h*x2)$, which neglects fractional portions. The result of the initial horizontal scaling from row0 and row1 of the buffer BUFFER1 is respectively stored in row5 and row6 of the buffer BUFFER2. The practical

5   implementation of the scaling process and the method of obtaining $w(n)$ are clear to those skilled in the art and will not be discussed here. However, one thing that should be mentioned is that the boundary conditions are treated as a mirror-extension process.

       Please refer to Fig. 7. Fig. 7 is a schematic diagram of mirrored data extension.

10   There are two options, and each option uses one row of the buffer BUFFER1 with the width of W as an example.

       In option 1:

       BUFFER1(-1) = BUFFER1(0),

       BUFFER1(W) = BUFFER1(W-1), and

15   BUFFER1(W+1) = BUFFER1(W-2).

       In option 2:

       BUFFER1(-1) = BUFFER1(0),

       BUFFER1(W) = BUFFER1(W-1), and

       BUFFER1(W+1) = BUFFER1(W-2).

20   Finally, in the last step of the initialization steps, the vertical index pointers y and y2 are both set to 0, where y is the vertical index counter for the memory SRC and y2 is the vertical index counter for the memory DST. The functions of pointers y and y2 will be clear in the following discussion.

25   In the group of the horizontal scaling steps, the first step is to re-arrange the buffer BUFFER2 as follows:

       BUFFER2(x2,0) = BUFFER2(x2,5)   if y = 0,

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BUFFER2(x2,0) = BUFFER2(x2,4)   if $y \neq 0$,

BUFFER2(x2,1) = BUFFER2(x2,5),

BUFFER2(x2,2) = BUFFER2(x2,6),

BUFFER2(x2,5) = BUFFER2(x2,4)   if $y \geq (H_d\text{-}7)$,

5   BUFFER2(x2,6) = BUFFER2(x2,3)   if $y \geq (H_d\text{-}7)$,

where x2 ranges from 0 to $(W_{new}\text{-}1)$.

After that, more rows of picture data are transferred from the SRC to the buffer
BUFFER1, such as:

BUFFER1(x,0) = SRC($2^{dn}*x, 2^{dv}(y+2)$),

10   BUFFER1(x,1) = SRC($2^{dn}*x, 2^{dv}(y+3)$);

and if $y < (H_d\text{-}7)$, then

BUFFER1(x,2) = SRC($2^{dn}*x, 2^{dv}(y+4)$),

BUFFER1(x,3) = SRC($2^{dn}*x, 2^{dv}(y+5)$),

where x ranges from 0 to $(W_d\text{-}1)$.

15   The horizontal scaling process is given as follows:

$$BUFFER2(x2,3) = \sum_{n=-1}^{2} BUFFER1(x1+n,0)*w(n), \text{ and}$$

$$BUFFER2(x2,4) = \sum_{n=-1}^{2} BUFFER1(x1+n,1)*w(n);$$

and if $y < (H_d\text{-}7)$, then

$$BUFFER2(x2,5) = \sum_{n=-1}^{2} BUFFER1(x1+n,2)*w(n), \text{ and}$$

20    $$BUFFER2(x2,6) = \sum_{n=-1}^{2} BUFFER1(x1+n,3)*w(n),$$

where x2 ranges from 0 to $(W_{new}\text{-}1)$ and x1 = floor(S_h*x2). That is, the horizontal scaling
results from row0 and row1 of the buffer BUFFER1 are saved to row3 and row4 of the
buffer BUFFER2, respectively. Also, if y is smaller than $(H_d\text{-}7)$, then the scaling results
from row2 and row3 of the buffer BUFFER1 are saved to row5 and row6 of the buffer

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BUFFER2.

In the group of vertical scaling steps, the first step is to let y1 = floor(S_v*y2). After that, if y1 satisfies y $\leq$ y1 < (y+4) and y2 satisfies y2 < H_{new}, then the vertical scaling

5 process is performed as follows:

$$DST(x2, y2) = \sum_{n=-1}^{2} BUFFER2(x2, y1 + n) * w(n),$$

where x2 ranges from 0 to (W_{new}-1). After the vertical scaling process, the vertical index pointer y2 is incremented by 1, i.e. y2 = y2+1. Finally, the process returns to the first step of the vertical scaling steps. On the other hand, if y1 does not satisfy y $\leq$ y1 < (y+4) or

10 y2 does not satisfy y2 < H_{new}, then the vertical index pointer y is increased by 4, i.e. y = y+4. After that, the range of y is verified; if y is smaller than (H_d-3), then the entire scaling process begins again from the first step of the horizontal scaling process. Otherwise, the scaling procedure has been accomplished and all processes are terminated.

15 In contrast to the prior art, the present invention provides a line-buffer scaling method that enables horizontal-scaling and vertical-scaling processes to use the same number of filter taps for achieving the best possible quality, while the buffer memory requirement is kept to be as small as possible and is proportional to the filter length. Therefore, this low-memory scaling method is suitable for the case when system memory

20 available is constrained.

Those skilled in the art will readily observe that numerous modifications and alterations of the device may be made while retaining the teachings of the invention. Accordingly, the above disclosure should be construed as limited only by the metes and

25 bounds of the appended claims.

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